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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,627	12/19/2005	Andrei Terechko	NL02 1504 US	8431

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
12/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,627	TERECHKO ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 9 October 2007 have been fully considered but they are not persuasive.

Regarding the non-statutory subject matter of claim 14, the examiner respectfully disagrees with applicant's assertion that the claim as a whole has not been considered, and offers further elaboration on the rejection.

The examiner notes that claim 1, which is the parent to claim 14, recites a "circuit arrangement". It is not immediately discernable to what statutory category a "circuit arrangement" belongs. A circuit arrangement could comprise, for example, the actual circuit itself, or a description of the circuit (i.e. a logic diagram, Verilog/VHDL code, a netlist derived from the compiled HDL code, or even merely a verbal description of the circuit elements, etc.). Nevertheless, for the sake of examination purposes, the invention of claim 1 was assumed to be a "machine" (to use the language of the statute), since the claims recite various hardware elements and the functionality thereof.

Claim 14 recites that the invention is a "program product comprising a hardware definition program defining the circuit arrangement of claim 1, and a signal bearing medium bearing the hardware definition program, wherein the signal bearing medium includes at least one of a transmission medium and a recordable medium." Based on this claim, it would appear the claim is not an machine, but rather an article of manufacture -- specifically, HDL code (i.e. Verilog or VHDL code) recorded on a "signal bearing medium". Applicant's specification discloses that signal bearing media is comprised of "recordable" and "transmission" media (pp. 10, lines 1-16), wherein recordable media comprises storage devices, and transmission media ostensibly comprises anything capable of transmitting data, including digital and analog

communication links. Based on applicant's distinction, one of ordinary skill in the art would readily conclude that transmission media would encompass such media as wireless transmission media and other types of propagated signals. Thus, based on applicant's own teachings, one embodiment of the invention would then be considered as comprising a wireless signal (a transmission type signal bearing medium) that encodes an HDL description of the circuit arrangement of claim 1. Although the examiner recognizes the claim includes recitation of a storage device (i.e. recordable media) upon which is recorded the HDL description (which by itself would be statutory, since storage devices are clearly articles of manufacture), the fact that the claim also includes recitation of non-statutory transmission media is sufficient to render the claimed invention as a non-statutory.

The examiner further wishes to note that the grounds for rejection do not rest upon applicant's claming of a signal bearing medium *per se*. Claims that recite signal bearing media, machine readable media, computer readable media, etc. may be allowable under 35 U.S.C. 101 provided that the specification clearly teaches that such media include articles of manufacture (storage devices, etc), and are not directed towards propagated signals or other media which cannot be properly categorized as process, machine, article of manufacture, or composition of matter. See MPEP 2106.01 [R-5], second paragraph, which states that functional descriptive material that is recorded on a computer readable medium may considered to be statutory. Note the further distinction in the following paragraph between computer-readable media and electromagnetic carrier signals; clearly, the separated listing of the two implies that computer-readable media are NOT meant to include such signals.

Regarding the rejection of applicant's claims over prior art, the examiner respectfully disagrees with applicant's arguments, and offers further elaboration on the rejection.

As stated in the previous office action, the Garg reference teaches aspects of applicant's claim relating to the structure of the register file and associated signals (address, data, clock), but does not teach the signal gating aspect of the applicant's invention. The Boice reference was cited as teaching aspects of applicant's claims relating to the gating of various signals for the purpose of reducing power consumption.

Boice teaches circuitry for isolating an on-chip array from input signal transitions. Fig. 7(a) of Boice clearly shows a clock signal [oscillator] and a enable signal which are inputs of an AND gate. The output of the AND gate is then fed into the clock input of the on-chip array. The operation of this circuit is self-evident. When the enable signal is logic low, the output of the AND gate is logic low regardless of transitions in the oscillator signal. When the enable signal is logic high, the output of the AND gate corresponds to the logic levels of the oscillator signal. Thus, the AND gate in Fig. 7(a) "gates off" the clock input for the on-chip array when the enable signal is logic low.

Similarly, Fig. 8 shows circuitry for isolating the on-chip array from new address/data signal values. AND gates 215 and 217, and OR gate 216 determine whether the address/data register value is updated based on the values of the Update and Quiesce signals 210 and 212. In the case where the Update 210 signal is logic low, the output of the AND gate 215 is also logic low, and new address/data information is prevented from being propagated to the address/data register, and ultimately the on-chip array. Thus, the AND gate 215 "gates off" the new address/data signals from the on-chip array when the Update signal is logic low.

Boice teaches an on-chip array which receives clock, address, and data signals. Garg teaches a register bank that receives clock, address, and data signals. Based on the disclosure of both Garg and Boice, it would have been obvious to one of ordinary skill in the art that the signal gating techniques of Boice could have been applied to Garg, with the predictable result

that gating the clock, address, and data signals of Garg's register bank would prevent unnecessary signal transitions in the register bank, thus providing the benefit of reducing power dissipation [col. 10, lines 25-27, 35-42].

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 14 recites program product comprised of a hardware definition program and a signal bearing medium that bears the hardware definition program, wherein the signal bearing medium comprises a transmission medium. Transmission media include digital and analog communication links as described by the applicant [specification pp. 10, lines 10-14], and as such are understood to include propagated signals. Propagated signals do not fall within any of the statutory categories for invention, nor do they represent a judicial exception with either a physical transformation or a useful, concrete, and tangible result. Therefore, the claimed subject matter is deemed to be non-statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 12, 13, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garg et al., U.S. Patent No. 5,493,687, in view of Boice et al., U.S. Patent No. 6,301,671 B1.

Regarding claim 1, Garg teaches a circuit arrangement comprising:

a register file partitioned into a plurality of banks [Fig. 1, register file 12, register bank 0..n], each bank including at least one register [Fig. 3, integer reg. set A], at least one clock input [CLK0], address input [Fig. 1, IEU mode integer switch lines 36 and 38 are used to access the register via offset addressing, col. 6, lines 1-8, 45-60], and data input [Fig. 3, write ports WA0, WA1]. Garg does not teach enable logic for gating off the clock, address, and data inputs.

Boice teaches a circuit comprising an on-chip memory array that receives clock, data, and address signals. The circuit of Boice prevents the clock, address, and data inputs of the on-chip memory array from transitioning when data is not read from or written to the array [Fig. 7a, 7b, 8 col. 10, lines 17-27, 35-67].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Garg and Boice by modifying Garg to prevent the clock, address, and data inputs of the register bank from transitioning when data is not read from or written to the register bank, as taught by Boice. Both Boice and Garg disclose circuits that store data values that also receive a clock, address, and data input signals. Boice teaches that in such circuits, power is often needlessly dissipated when input signals are transitioning even though data is not being read or written [col. 1, lines 26-40]. Boice additionally teaches that it would be desirable to prevent spurious power dissipation by preventing input signal transitions when they are not needed [col. 10, lines 25-27, 35-42]. The teachings of Boice would improve the circuit of Garg by preventing the input signal transitions when they are not needed, and thus decreasing power consumption.

Therefore, one of ordinary skill in the art would have been motivated by Boice's disclosure to modify the circuit of Garg in light of Boice's teaching.

Regarding claim 2, official notice is taken that it would have been obvious to one of ordinary skill in the art to implement the register file using a CMOS latch or flip-flop, as those are standard components used in the implementation of registers.

Regarding claim 3, Boice teaches a plurality of enable circuits coupled to the array, each circuit configured to gate off each clock, address, and data input for the array in response to an enable signal [Fig. 7a, enable, Fig. 8, quiesce].

Regarding claim 4, Boice teaches a plurality of gates that are used to gate the clock, address, and data signals [Fig. 7a, Fig. 8] responsive to an enable signal. Additionally, it is noted by the examiner that logic gates are inherently comprised of transistors.

Regarding claim 5, Garg teaches output select logic coupled to the register bank [Fig. 3a, multiplexers coupled to the read outputs of register bank in Fig. 3].

Regarding claim 6, Boice teaches that the enable logic dynamically determines when the array is unused and generates an enable signal accordingly [col. 10, lines 19-22].

Regarding claim 7, Boice teaches that the enable logic comprises an address decoder that generates the enable signals based on an updates address [col. 10, lines 46-50].

Regarding claims 12 and13, Garg teaches that the circuit is a processor disposed on an IC [Fig. 1, RISC processor].

Regarding claims 15-19, the combination of Garg/Boice teaches the circuit of claims 1-7, and also the method implemented by the claimed circuit. Additionally, the examiner notes that Boice discloses a plurality of functional blocks each with its own memory array [col. 10, lines 11-14], wherein the array for an individual functional block is selectively enabled or disabled [col. 10, lines 19-22, col. 11, lines 1-6] . This is an analogous arrangement to Garg,

wherein Garg teaches a plurality of register banks to which the teachings of Boice would be applied in the manner similar to that of the plurality of functional blocks in Boice.

Claims 8-10, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garg/Boice as applied to claims 1-7, 12, 13, and 15-19 above, and further in view of Gupta et al., U.S .Patent No. 5,996,083.

Regarding claim 8, Garg/Boice teaches the circuit arrangement of claim 1, but does not teach stored power mode state information that is used to generate the enable signal.

Gupta teaches a system comprised of a plurality of functional blocks, wherein the power consumption of an individual functional block is selectively controlled based on a power control register field that stores a value for that particular functional block [Fig. 2, col. 3, lines 40-51, col. 5, lines 60-67].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Garg/Boice with Gupta by implementing the power control register and associated prediction logic of Gupta in the system of Garg/Boice. Garg/Boice and Gupta are directed towards systems wherein functional blocks may be selectively enabled or disabled in order to reduce power consumption. In particular, Boice teaches that an enable signal is generated for a particular memory array based on a determination of whether that array is needed or not [col. 10, lines 19-27, 35-50]. However, Gupta teaches that it would be desirable to look further ahead into the execution of a processor in order to give advance warning of whether or not a given functional block will be needed [col. 3, lines 1-12, 44-51]. The teachings of Gupta would have improve the system of Garg/Boice by providing the ability to predict when a given functional block would be needed. Therefore, one of ordinary skill in the art would have been

motivated by Gupta's teachings to further modify the circuit arrangement of Garg/Boice in the manner suggested by Gupta.

Regarding claim 9, Gupta teaches that the power mode state information is stored in the power control register, and is updated by a power control instruction resident in program code executed by the processor [updated by software, col. 5, lines 63-64].

Regarding claim 10, Gupta teaches that the power control register is a power modes register [col. 9, lines 37-39, power control register indicates power modes].

Regarding claims 20 and 21, the combination of Garg/Boice/Gupta teaches the arrangement of claims 8-10, and also the method implemented by the claimed circuit.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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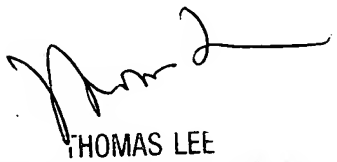

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